Claims 1-2 and 7-8 are rejected under 35 U.S.C. §103 as being unpatentable over the admitted prior art in view of Gutierrez (U.S. Patent No. 5,056,749).

The admitted prior art as shown in Figs. 1A-1B does not disclose or teach a two-step deposition process to achieve better step coverage of the metal layer (see the present specification, from page 4, the last paragraph to page 5, the second paragraph).

Gutierrez discloses a method of fabricating interconnect layers on an integrated circuit chip using seed-grown conductors. Gutierrez does not disclose or teach a method for filling contact holes in a two-step deposition process to achieve a better step coverage of a two-layer structure. In fact, Gutierrez uses a four-step deposition process for a two-layer structure. As disclosed in FIGs. 1-6, the recess 50 (or 52) needs two-step to be entirely filled. The first step is to deposit an initial layer of conductive material by a process which deposits conductive material selectively where seed material (30,32) is exposed (see column 3, lines 57-61). The chip is immersed in an atmosphere of tungsten fluoride gas. The gas reacts with the silicon seed material (30,32) to form the tungsten according to the formula disclosed in column 3, line 67. The solid tungsten is deposited, and the silicon fluoride gas is dispersed (see column 3, line 62 to column 4, line 4). The result of the first step, as shown in FIG. 5, is that the bottom of each recess 50 (or 52) has a layer of tungsten 60 (or 62). Accordingly, the recess is not entirely filled with the metal material (e.g.

tungsten) as claimed in claim 1. To entirely fill the recess, a second step is accomplished by introducing hydrogen gas into the atmosphere of tungsten fluoride gas. The hydrogen and tungsten fluoride react according to the formula disclosed in column 4, line 28. This reaction occurs in the presence of solid tungsten as a catalyst. The reaction results in the selective deposition of tungsten in locations where tungsten was previously deposited by the selective deposition on the seed material (see column 4, lines 30-34). Gutierrez further discloses, "All of the contact vias 218, 222, 224, 226, and 228 and metal interconnection lines 212, 214, 216, and 220 are formed by the above-described process" (see column 5, lines 18-21). Accordingly, to make a two-layer structure, such as layers 232-234 as shown in FIG. 8 of Gutierrez, two steps are needed to fill via 220, and another two steps are needed to fill via 218. Thus, Gutierrez teaches away from the claimed invention.

In fact, Gutierrez's process does not allow a contact hole to be entirely filled by one step as claimed in claim 1. In the first step, Gutierrez discloses that the reaction of tungsten fluoride with silicon will slow and eventually stop after the deposited conductive material (tungsten) is thick enough to prevent contact between the tungsten fluoride and the silicon (see column 4, lines 5-8), which also in one sense, is not practical or recommended being used for making contact due to the left over of seed material. Gutierrez further discloses that the volume of silicon consumed by this reaction is greater than the volume of tungsten deposited (see column 4, lines 8-10). For these two reasons, Gutierrez concludes that this reaction

probably will not deposit, by itself, sufficient tungsten to fill the recesses 50 and 52 (see column 4, lines 10-12). This is contrary to the claimed invention and also teaches away from the claims.

Furthermore, Gutierrez discloses that via 226 is formed directly onto the silicon substrate using the substrate as the seed (see column 5, lines 23-24), and that the seed 30 or 32 is consumed by the reaction with the tungsten fluoride (see column 3, line 67). Had one applied Gutierrez's process to the claimed invention, the gate electrode (e.g. 5 which is made of polysilicon in one embodiment) or N+ or P+ junction layer (e.g. 2 in one embodiment) would have been consumed similarly. Evidence can be found in FIG. 8 of Gutierrez, e.g. contact vias 228 and 226, where silicon 114 and 116 (shown in FIG. 7) are consumed. This is undesirable and contrary to the claimed invention (see the embodiment shown in Figs. 2B-2D), in which the gate electrode 5 and the layer 2 are not consumed.

Therefore, Applicant respectfully submits that claim 1 patentably distinguishes over Gutierrez. Claims 2 and 7-8 which are dependent from claim 1 are also patentable.

In view of the above, it is respectfully submitted that the present application is in a condition for allowance. Reconsideration of the present application and a favorable response are respectfully requested.

If a telephone conference would be helpful in resolving any remaining issues, please contact the below signed at 612-336-4733.

Respectfully submitted,

MERCHANT, GOULD, SMITH, EDELL,
WELTER & SCHMIDT, P.A.
3100 Norwest Center
90 South Seventh Street
Minneapolis, Minnesota 55402

By _____
Min Xu
Registration No. 39,536
AX/mas